WHAT IS CLAIMED:

1. A receiver comprising:

an A/D converter for converting received analog signals to a digital signal data stream, wherein the digital signal data stream includes symbols separated by guard segments;

an I/Q demodulator for producing a first set of complex I and Q components from the digital signal data stream;

a guard segment length detector using the first set of I and Q components;

an extractor for identifying and removing the guard segments of the detected length from the digital signal data stream; and

an FFT demodulator for demodulating the symbols of the digital signal data stream to produce second sets of complex I and Q components.

2. The receiver according to claim 1, wherein the FFT demodulator demodulates two symbols at one time to produce the second sets of complex I and Q components.

3. The receiver according to claim 2, wherein the FFT demodulator operates in one of a 4K mode for a 2K requested mode and 16K mode for an 8K requested mode.

4. The receiver according to claim 1, including a first carrier signal offset estimator and a first symbol synchronizing signal generator, each using the first set of I and Q components, to estimate the offset of the carrier signal and adjusting the A/D converter and to generate a symbol synchronizing signal for the extractor, respectively, at least during an initialization phase of the receiver.

5. The receiver according to claim 4, wherein I/Q demodulator, the guard segment length detector, the first carrier signal offset estimator, and the first symbol synchronizing signal generator operate only during the initialization phase of the receiver.

6. The receiver according to claim 4, including a second carrier signal offset estimator and a second symbol synchronizing signal generator, each using the second sets of I and Q components from the FFT demodulator, to estimate the offset of the carrier signal and adjusting the A/D converter and to generate a symbol synchronizing signal for the extractor, respectively, at least after an initialization phase of the receiver.

7. The receiver according to claim 1, including a processor programmed to operate as the I/Q demodulator, the guard segment length detector, the extractor and the FFT demodulator.

8. The receiver according to claim 1, wherein the FFT demodulator is an orthogonal frequency division multiplexing demodulator.

9. The receiver according to claim 1, wherein the receiver is a digital video broadcasting receiver.

10. The receiver according to claim 1, wherein the receiver includes at least two antennas each connected to a respective receiver front-end and A/D converter.

11. The receiver according to claim 10, wherein the at least two antennas are orthogonally positioned and the receiver front-end includes a phase shifter.